

A SEMICONDUCTOR TESTING DEVICE HAVING A DETACHABLE NEST ANVIL

ABSTRACT

5 A semiconductor testing device having a nest for holding an integrated circuit during testing. The nest comprises a plate having a front side and a back side, a cavity in the plate for receiving an integrated circuit having a plurality of pins, a channel for receiving therein an anvil, and an anvil detachably engaged within the channel, positioned to engage the pins of the integrated circuit and to
10 maintain the pins in alignment.

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